SPECIFICATION

Please replace the abstract beginning on page 11 of the preliminary amendment filed October 31, 2003 with the following:

The method and apparatus feature detecting an interrupt service request; ~~inserting interrupt servicing instructions responsive to the interrupt service request into an instruction queue mechanism in such manner that the inserted interrupt servicing instructions intervene mainline program instructions within a queue mechanism thereby allocating core processor bandwidth between the inserted interrupt servicing instructions and the mainline program instructions;~~ storing into an instruction cache interrupt service instructions in response to detecting the interrupt service request; and fetching instructions from the instruction cache into an instruction stream sequence, the instruction stream sequence including mainline program instructions and the interrupt service instructions resulting in allocating core processor bandwidth between the interrupt servicing and mainline program instructions while executing the instruction stream sequence based on an interrupt priority; and processing ~~the~~ instructions within the instruction ~~queue mechanism~~ stream sequence including the mainline program instructions and the inserted interrupt servicing instructions. ~~By doing so, core processor bandwidth allocation between the mainline program instructions and the inserted interrupt servicing instructions is achieved by concurrent in-line staging of the same within the instruction queue mechanism.~~ The method and apparatus further feature recycling of executed micro-ops and detecting imminent context switch for interrupt service instruction preparation.